REMARKS

Reconsideration and allowance of the present application are respectfully requested. Claims 1-9 remain pending in the application. By this Amendment claim 1 is amended.

In numbered paragraph 2, pages 2-5 of the Office Action, independent claim 1, along with various dependent claims, is rejected as being unpatentable over U.S. Patent 6,609,167 (Bastiani et al.) in view of U.S. Patent 6,718,413 (Wilson et al.). In numbered paragraph 3, page 5 of the Office Action, dependent claim 9 is rejected as being unpatentable over the Bastiani et al. patent, in view of the Wilson et al. patent, and further in view of U.S. Patent 5,555,430 (Gephardt et al.). These rejections are respectfully traversed.

Applicants have disclosed a transceiver configured for use with a multi-tier system bus that allows for the flow of information to be managed among plural processors by connecting processors within modules on a local bus, which is then connected to the system bus by way of a gateway (e.g., paragraph [0015). As exemplified in Fig. 2, a bus interface utilizes a transmitter and receiver that operate between the local processor bus 202 and the system bus or module bus 204. The bus 204 can be either a system bus 102 or a module bus 122 as shown in Figure 1. The local processor bus 202 can be a bus connecting a bus interface device 128 to components within the same node of the module, such as processors and memory, or, in the case of the sensor interface, internal processors and memory (e.g., paragraph [0084]). As set forth in Applicants' previous Response, Applicants have disclosed that two basic types of operations are supported, including DMA operations and control operations (e.g., paragraph [0093]).

The foregoing features are broadly encompassed by claim 1, which recites a transceiver for use within a multi-tier system bus configuration, including, among other features, means for buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA) operations for forward to a local processor bus; and means for buffering instructions transmitted via the local processor bus to provide a separate transmit buffering of control actions from DMA operations to be transmitted to the system bus; wherein access to the multi-tier system bus is arbitrated such that control actions preempt DMA operations.

The Examiner asserts at page 3 of the Office Action that the Bastiani et al. patent teaches "means for buffering instructions received and transmitted...via the system bus...to provide a separate buffering of control actions...from DMA operations." Applicants respectfully disagree with the Examiner's ultimate conclusion.

The Bastiani et al. patent does not relate to a transmitter and receiver that operate between a local processor bus and a system bus. Rather, what is shown in Fig. 41 of the Bastiani et al. patent is an advanced serial protocol (ASP) controller connected between a PCI interface (352) on one side, and a plurality of serial transceivers (372). These transceivers (372) are ENDEC transceivers for serial data transmission (col. 48. lines 62-65). There is no teaching or a suggestion of at least 1) a transceiver described within a multi-tier system bus having a local processor bus and a system bus; and there is no suggestion of 2) a separate buffering of control actions from DMA operations within such a multi-tier system bus architecture. The Bastiani et al. patent would not have taught or suggested specifically means for

buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA) operations for forward to a local processor bus; and means for buffering instructions transmitted via the local processor bus to provide a separate transmit buffering of control actions from DMA operations to be transmitted to the system bus, as recited in claim 1. Further, as admitted by the Examiner, the Bastiani et al. patent "does not explicitly teach wherein access to the multi-tier system bus is arbitrated such that control actions preempt DMA operations."

The Wilson et al. patent does not cure the deficiencies of the Bastiani et al. patent. As set forth in Applicants' previous Remarks of record, the Wilson et al. patent merely relates to SCSI devices contending for a bus in operation 606 to allow one SCSI device to transfer data to the host adapter in the operation 614 (col. 10, lines 57-65). The Wilson et al. patent would not have taught or suggested specifically means for buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA) operations for forward to a local processor bus; and means for buffering instructions transmitted via the local processor bus to provide a separate transmit buffering of control actions from DMA operations to be transmitted to the system bus, as recited in claim 1. Further, the Wilson et al. disclosure is not specific to an arbitration involving access to a multi-tier system bus such that control actions preempt DMA operations, as recited in claim 1.

The Gephardt et al. patent does not cure the deficiencies of the Bastiani et al. patent and the Wilson et al. patent. The Gephardt et al. patent was applied for its disclosure of interrupt management in a multiprocessing system (col. 22, line 61

through col. 23, line 17). However, the Gephardt et al. patent would not have taught or suggested specifically means for buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA) operations for forward to a local processor bus; and means for buffering instructions transmitted via the local processor bus to provide a separate transmit buffering of control actions from DMA operations to be transmitted to the system bus, as recited in claim 1. Further, the Gephardt et al. disclosure is not specific to an arbitration involving access to a multi-tier system bus such that control actions preempt DMA operations, as recited in claim 1.

For the foregoing reasons, Applicant's claim 1 is allowable. The remaining claims depend from independent claim 1 and recite additional advantageous features which further distinguish over the documents relied upon by the Examiner. As such, the present application is in condition for allowance.

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the application is in condition for allowance and a Notice of Allowance is respectfully solicited.

Respectfully submitted,

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